### Unified Toolkit for Compositional Design

**Building Blocks**

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<th>Devices Ctrl. API</th>
<th>Power Ctrl. API</th>
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<td>Specialized Accelerator</td>
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**Supervised High Level Synthesis**

- Pareto-optimal implementations and composition of accelerator’s sub-components [3]
- Sub-components’ communication optimization [4]
- Scratchpad micro-architecture optimization and local memory reuse (ongoing work)

**Virtual Platform**

- Full System: runs target OS, software app and device drivers
- Parallel simulation of heterogeneous concurrent components

**Methodology for Evaluation and Design Space Exploration**

- Target Applications
  - Which kernels will benefit the most from hardware acceleration?
  - Hardware vs. software execution
  - Which is the optimal data token size? Scratchpad size vs. communication overhead.
  - How much parallelism can be exploited? Performance vs. power
  - Which is the optimal operation point? Voltage and frequency scaling

- Constraints
  - Timing requirements, area, power and energy budget
  - Available IPs
  - I/O bandwidth and pin count

- Run HLS
  - IP refinement
  - Integrate Prototype refinement
  - Sweep models parameters
  - IP optimization
  - Resource sharing

- Parameters projection for target system
  - Runtime - Operations count
  - Power - Energy
  - Cost of communication and I/O

**CARGO Simulation**

Design Space Exploration engine

- Prototype full system performance
- Area, power and latency

**System Integration and Implementation**

- Embedded Scalable Platform Instance
  - Components selection
  - Communication interface and wrappers selection
  - Drivers and software stack finalization

**References**

[2] N. Sturikov et al. A 2.5D integrated voltage regulator using coupled magnetic core inductors on silicon interposer delivering 10.84 mV/mm^2. ISSCC 2011

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Disclaimer: Any opinions, findings and conclusions or recommendations expressed in this material are those of the authors and do not necessarily reflect the views of DARPA.